REMARKS

Reconsideration and allowance are requested.

A new, more descriptive title and an amended abstract are submitted as requested by the Examiner. Withdrawal of the objections to the title and abstract are requested.

Claims 1-3, 7,8, 10, 11, and 15 stand rejected for anticipation under 35 U.S.C. §102 based on EP 1014626. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986).

EP 1014626 fails to teach a receiver unit transmitting over a databus to a transmitting unit a blocking sequence that is used for collision detection as recited in independent claims 1 and 9. The Examiner admits this deficiency in paragraph 11 of the office action. The anticipation rejection should be withdrawn.

Claims 9 and 12-14 stand rejected under 35 U.S.C. §103 as being unpatentable based on EP 1014626 and USP 6,625,163 to Shideler. This rejection is respectfully traversed.

Shideler discloses an application module that is part of an electronic assembly including a controller module. The application module is coupled to a backplane bus. The backplane includes a differential bus with a TX and RX data signal, a differential clock signal, and a separate, single- ended collision detection line. The application module comprises differential bus transceivers that are controlled by differential bus control logic on the application module.

The control logic compares data bits received over a collision detection line with the data bits the application module originally transmitted. If the data is not the same, a collision has occurred and the control logic places the bus transceivers into a high impedance state.

The independent claims are not directed to collision detection, which is the feature the Examiner identifies as being added to EP 1014626. Instead, the claims "control a data flow, including an overflow condition at said receiver unit, using a control data sequence output on said databus," as recited in claim 1, and "control a data overflow condition at said receiver unit" using a control data sequence that "includes a collision detection blocking sequence which alters a transmission mode of said at least one transmitting unit upon reception of said control data sequence," as recited in claim 9. Neither EP 1014626 nor Shideler disclose or contemplate using a collision detection blocking data sequence for the entirely different purpose of controlling data overflow at the receiver. So even if Shideler could be combined with EP 1014626, that combination fails to teach all of the features in the independent claims.

In addition, the Examiner's combination of EP 1014626 and Shideler is improper as a matter of law. The Examiner articulates that it would have been obvious to these references because "both the prior art systems are analogous to use HDLC protocol and the above feature is a straightforward possibility for which one of ordinary skill in the art at the time the invention was made would select in accordance with circumstances without the exercise of inventive skill." But this rationale is nothing more than an "obvious to try" hindsight approach to obviousness.

The Federal Circuit has consistently held that there must be "some teaching, suggestion, or motivation to combine references." *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998). "Stated another way, the prior art as a whole must 'suggest the desirability' of the combination." *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004). Just because something is feasible does not

make it desirable. The Federal Circuit mandates that "motivation to combine requires the latter [desirable]." *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 (Fed. Cir. 2000). A "straightforward possibility" as posited by the Examiner relates to feasibility not desirability.

In addition, the Federal Circuit *requires* consideration of the problem confronted by the inventor in determining whether it would have been obvious to combine references in order to solve that problem. *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 935 (Fed. Cir. 1990). Indeed, the Examiner must show reasons why one of ordinary skill in the art, confronted with the same problem as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. See *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998).

The *Rouffet* Court warned against "rejecting patents solely by finding prior art corollaries for the claimed elements" because that would "permit an Examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art." *In re Rouffet*, 149 F.3d at 1357. That approach was found by the Federal Circuit to be "an illogical and inappropriate process by which to determine patentability." *Sensonics v. Aerosonic Corp.*, 85 F.3d 1566, 1570 (Fed. Cir. 1996). The Examiner fails to show that either reference addresses the same problem as the inventors in this case. Indeed, the combination requires an additional line for collision detection be provided, which is something the inventors in this application specifically wanted to avoid. See page 2, line 37+ and Figure 2.

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
John R. Lastova
Reg. No. 33,149

JRL:maa
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100